REMARKS

This Reply is responsive to the Final Office Action dated November 1, 2006 ("Office Action"). This Reply is accompanied by a petition for a one-month extension of time along with an authorization to charge the required statutory fees. A rule 131 Declaration (the "Declaration") executed by inventor Eisenstadt accompanies this reply. The Commissioner is also expressly authorized to charge any other fees to Deposit Account No. 50-0951 to maintain the pendency of this application.

On page 2 of the Office Action the following objection was asserted:

> 2. Claim 12 is objected to because of the following informalities: it lacks antecedent basis (i.e. "said at least one intermediate voltage"). Appropriate correction is required.

In this Reply, claim 12 has been amended ***solely*** to overcome the objection noted above. Based on this amendment, the objection to claim 12 is now overcome.

Claim 29 was rejected under 35 U.S.C. § 112, second paragraph as being indefinite. In this Reply, claim 29 has been cancelled. Based on this amendment, the rejection is now overcome.

Regarding claim rejections based on cited art, claims 1, 3, 6, 9, 10, 12, 13, 17, 19, 22, 25 and 26 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0129888 to Kannan et al. (Kannan). Claims 1, 2, 5, 7

and 8 were rejected under 35 U.S.C. §102(a) as being anticipated by Japanese Patent Publication 2002-101558 to Suzuki (Suzuki). Claims 17, 18, 21, 23 and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Suzuki. Claims 4, 11, 20 and 27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of U.S. Patent No. 6,411,531 to Nork et al. (Nork) and U.S. Patent No. 6,633,494 to Roohparvar et al. (Roohparvar). Claims 14 and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of the publication "Switched-Capacitor DC-DC Converters for Low-Power On-Chip Applications" by Maksimovic et al. (Maksimovic).

Claim Amendments

Independent claims 1 and 17 have been amended by including the further limitation that the plurality of outputs of the DC to DC converter provide a plurality of supply voltages having voltage levels greater than the supply voltage. Claims 1 and 17 have also been amended to further clarify that a modified time-varying signal output by the processing circuitry is scaled to a voltage level of one of the plurality of output voltages being used as a supply voltage by the processing circuitry. Explicit support for scaling the output levels according to the supply voltage of the processing circuitry for a modified time-varying signal can be found on page 13, lines 6-13, and page 15, lines 10-16. In particular these sections discuss the using an output supply voltage of the DC to DC converter as the supply voltage for the processing circuitry. The paragraphs that follow discuss that the output of the exemplary processing circuitry in FIG. 5 and FIG. 6

allow the voltage levels of V_{out} (output signal for the processing circuit) to proportionately swing from ~0 Volts to a supply voltage level for the processing circuitry. Therefore, as recited in claims 1 and 17, the voltage levels for the output signals of the processing circuit would be scaled proportionately from ~0V to the voltage level of one of the plurality of output supply voltages being used as a supply voltage for the processing circuitry. No new matter has been added by the Amendment.

Applicant's Invention Predates Suzuki

As noted in the Office Action, independent claim 1 was rejected under 35 U.S.C. §102(a) as being anticipated by Suzuki. Furthermore independent claim 17 as rejected under 35 U.S.C. §103(a) as being unpatentable over Suzuki. Applicant respectfully disagrees that Suzuki, afforded a filing date of April 5, 2002, alone or in combination with any other reference of record, fails to disclose, suggest, or render obvious all of the features recited in the rejected claims. However, Applicant respectfully submits that the issue is moot because Applicant's invention predates the April 5, 2002 filing date afforded to Suzuki, as evidenced in the Declaration provided herewith.

Applicant herewith provides a Rule 131 Declaration executed by inventor Eisenstadt which evidences a date of conception prior to the April 5, 2002 filing date of Suzuki, along with evidence of diligence until the filing date of the present application. The Declaration is accompanied by a copy of a complete copy of a University of Florida

Invention Disclosure regarding the present case signed by inventor Eisenstadt on March 18, 2002 (Marked as Exhibit "A").

The Invention Disclosure demonstrates proof of conception and enablement for the claimed subject-matter of Applicant's invention prior to April 5, 2002, the date afforded to Suzuki as a reference. Once a University of Florida invention disclosure form is submitted, the disclosure is reviewed by the Office of Technology and Licensing to determine whether to prepare an application based upon the submitted disclosure. Upon reaching a decision to prepare an application, an outside counsel is generally selected to prepare the application.

A first outside counsel was authorized to file a patent application based on the present disclosure on March 28, 2002. The invention disclosure was subsequently transferred to a second outside counsel, the undersigned. The undersigned were authorized to file a patent application based on the present invention on May 31, 2002. Evidence of such authorization to file a patent application by first counsel and the undersigned is provided in Exhibits "B", "C", and "D", accompanying this reply.

Exhibit "B" is a misdated letter received by the undersigned authorizing the undersigned to file a patent application based on the present disclosure. Exhibit "C" is an e-mail message indicating the reason for the incorrect date on the letter. Exhibit "C" evidences that the letter forwarded to the undersigned was originally prepared for first

outside counsel, who were authorized to file the patent application on March 28, 2002. The date was inadvertently left unchanged when the authorization was forwarded to the undersigned. Exhibit "D" is a copy of the corrected letter received by the undersigned authorizing the undersigned on May 31, 2002 to file a patent application based on the present disclosure.

The undersigned prepared a draft of the application that was iteratively reviewed by the named inventor until such time that the inventor was satisfied that the application sufficiently detailed the inventive concepts detailed in the disclosure, at which time the provisional application was filed with the U.S. Patent and Trademark Office on October 2, 2002. Regarding diligence, the Declaration provides sworn testimony in Sections 7 and 8 that the inventor exercised reasonable diligence from a time prior to April 5, 2002 to the October 2, 2003 filing date of the present application.

The undersigned prepared the Application consistent with long-established professional practices. According to these established practices, outside counsel prepares cases on a first-in, first-out basis unless a particular case is associated with a bar date, in which event the case is granted priority within the work queue. The undersigned followed this professionally-accepted practice in preparing the Application in this case.

Applicant respectfully submits that his earlier conception coupled with reasonable diligence from a date prior to the effective date of Suzuki precludes using Suzuki as the

basis for a rejection for any of the claims. Accordingly, Applicant respectfully submits that each of independent claims 1 and 17 now defines over the references of record, as discussed below.

Aspects of the Claimed Invention

Prior to discussing the cited art, it may be useful to reiterate certain aspects of Applicant's invention. Claims 1 and 17 of the present invention recite an integrated circuit comprising a DC to DC converter that provides a plurality of output supply voltages for other integrated circuit components having different voltage level input requirements. In particular, the plurality of output supply voltages are at levels higher than a supply voltage provided to the integrated circuit in claims 1 and 17. Furthermore, claims 1 and 17 further recite that the processing circuitry can receive as an input a time varying signal and at least one of the output supply voltages in order to produce a time varying signal scaled to a output supply voltage level. As stated in the Background of the Invention, a difficulty with combing various integrated circuits is that the voltage levels of the integrated circuits needed for a design are not always compatible. The claimed invention overcomes this difficulty by providing a single integrated circuit with a single power supply that can scale signals upward to provide other integrated circuits with supply voltage levels and input signal levels which function in higher voltage ranges.

The Claims Define over the Cited Art

In the Office Action, claims 1, 3, 6, 9, 10, 12, 13, 17, 19, 22, 25 and 26 were rejected under 35 U.S.C. §102(e) as being anticipated by Kannan et al. (US 2004/0129888). Kannan discloses a low cost, digital dosimeter for measurement of radiation dose from ionizing X and Gamma radiation of energy greater that 60 KeV, including means for converting, amplifying, filtering, calibrating electrical impulses generated from ionizing radiation detected by the dosimeter. On pages 2 and 3 of the Office Action, it is asserted that:

> 6. Claims 1, 3, 6, 9, 10, 12, 13, 17, 19, 22, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Kannan et al. (2004/0129888). Kannan teaches a plurality of integrated circuits (10-12, among others) on a board (Fig. 1). The integrated circuits require a plurality of different supply voltage levels and signals at respective inputs for operation. He also teaches DC-DC converter (6) for receiving a supply voltage and producing a plurality of amplified output voltage pulses (of varying amplitude). He also teaches a processing circuit (9) for receiving an output voltage from the converter and a time-varying input signal (from 6 and/or 8A) and produces a modified time-varying signal, in the form of voltage pulses (of varying amplitude). The varying parameter is the voltage level. He also teaches a plurality of output voltages (from 6) coupled to a plurality of integrated circuits (9-12) and a plurality of outputs (from 9) coupled to said inputs of a plurality of integrated circuits (10-12). The processing

Applicant respectfully disagrees and asserts that Kannan, separately or in combination with any other reference of record, fails to disclose or suggest or render obvious each and every element as recited in the claims. Applicant directs attention to the portion of Kannan cited by the Office Action, where Kannan describes FIG. 1:

[0088] This is the block diagram of the digital pocket dosemeter embodying the invention. A radiation dose of 1 μSV corresponds to approximately 20 pulses delivered by the detector 1 over and above the electrical noise pulses. The detector is applied a reverse bias (The detector has two electrodes, anode & Cathode. Reverse bias means that anode is given a negative potential with respect to cathode) through resistor 5. The pulses from the detector are amplified by the pulse amplifier 6 and are fed to a discriminator 9. The discriminator passes to its output only those pulses of height more than the threshold voltage applied to it. The threshold voltage adjusted through resistor 7 and potentiometer 8, to cut off the noise pulses. A waveform generator circuit 8A produces an approximately linear ramp of height 1V at a repetition rate of 500 Hz. The ramp is superimposed on the discriminator threshold voltage through capacitor 8B. The pulses at the output of the discriminator are fed to a programmable divider 10. The programmable divider can be adjusted so as to produce one pulse at the output for every 20 pulses at the input so that 1 count corresponds to 1 μSv at the output of the programmable divider. These pulses are then fed to a 6-digit electronic counter 11 which is incremented by every pulse and the total number of pulses received by the counter up to any instant of time remains stored in the counter. The contents of the counter are displayed by the display device 12, which is a seven-segment, 6 digit LCD display. The entire circuitry is powered by a 6V Lithium battery 3. The battery voltage is regulated to 4V by a voltage regulator 3B and applied to the circuitry. The condition of the battery is monitored by a battery low indicator circuit 4. When the battery voltage falls below the acceptable limit LED 2 starts flashing. The switch 3A provides the means of switching the dosemeter 'On' and 'Off'.

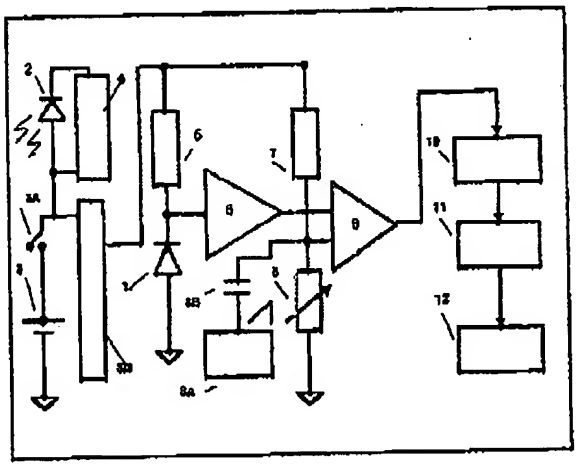

FIG. 1

First, Kannan fails to disclose providing a plurality of varying output voltages to a plurality of integrated circuits. As shown above in paragraph [0088] of Kannan, Kannan explicitly provides a signal of 6V from a single battery regulated to 4V. Kannan further states that the single 4V signal is used to power all the integrated circuits in dosimeter

circuit. Nowhere does Kannan disclose or suggest providing multiple supply voltages to a plurality of integrated circuits. Therefore, the plurality of integrated circuits in the circuit of Kannan must all necessarily be able to operate at a single voltage supply level, including the asserted processing circuitry (9). In contrast, the claimed invention utilizes a single integrated circuit to provides a plurality of output supply voltages which can be coupled to a plurality of integrated circuits operating at different voltage levels, a motivation for the claimed invention. Furthermore, the processing circuitry of the claimed invention can be configured to operate at a supply voltage that is different from the supply voltage of the DC to DC converter.

Second, Kannan fails to disclose a DC to DC converter, as recited in the claimed invention. It is asserted in the Office Action that component (6) in FIG. 1 of Kannan is equivalent to the DC to DC converter of the claimed invention. Applicant respectfully disagrees. The output of the pulse amplifier (6) in Kannan is specifically limited to generating signals having only an amplified voltage, as disclosed in paragraphs [0085], [0088], and [0093]. As such, Applicant asserts that ***Kannan discloses component (6) in FIG. 1 as an amplifier, not us a converter.*** For example, in paragraph [0089], Kannan discloses that (1), (5), and (6) in FIG. 1 comprise a "detector-amplifier" portion. Kannan further discloses specific structure and function for the components of the detector-amplifier, as shown in FIG. 3 and described in paragraph [0093], reproduced below:

[0093] This is the detector and amplifier part of the circuitry. The detector 16 is reverse biased by connecting the cathode to VCC (a regulated voltage obtained using a voltage regulator described in FIG. 1) and the anode to circuit common through resistor 17. The pulses from the detector are fed to the charge-sensitive pulse amplifier comprising of CMOS amplifier 20A, input capacitor 18, feed back capacitor 19 and resistor 21. The pulses are amplified by three more stages of amplifiers comprising of resistors 21, 23, 25 & 27 and CMOS amplifiers 20B, 20C & 20D

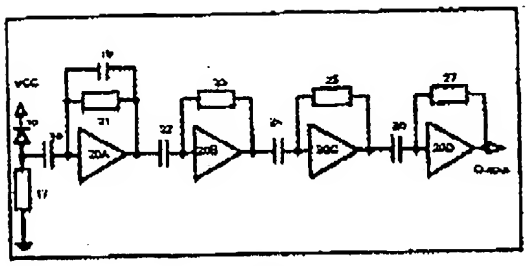

FIG. 3

As shown above in FIG. 3 of Kannan and as described in paragraph [0093], the amplifier (6) of Kannan is a multistage amplifier (components (20A), (20B), (20C), and (20D)), ***for only amplifying*** electrical impulses emitted by the detector portion. Applicants respectfully assert that at the time of filing of the application, one of skill in the art would have known that ***an amplification circuit would have only allowed a signal to be amplified to a level below or equal to the supply voltage, not to a voltage level higher than the supply voltage.*** Furthermore Kannan does not disclose or suggest that different power supplies are applied to each amplification stage. Therefore, since Kannan only provides amplification and a single supply voltage for the entire circuit, Kannan cannot provide voltage levels from the DC to DC converter exceeding the power supply voltage. In contrast, the DC to DC converter of the claimed invention provides a plurality of output supply voltages having a voltage level greater than the supply voltage of the integrated circuit.

Third, the circuit of Kannan fails to disclose or suggest that the asserted DC to DC converter (6) provides a voltage supply for the asserted processing circuitry (9). As

shown above in paragraph [0083] and FIG. 1 of Kannan, the amplifier (6) provides a signal to as an input to the discriminator (9), but not as the voltage supply. Nowhere does Kannan disclose or suggest that signals, whether scaled or amplified, from the amplifier (6) would be provided to voltage supply node of the discriminator (9) of Kannan. Rather as previously discussed, all elements of the circuit in Kannan utilize the same supply voltage. In contrast, the inputs of the processing circuitry in the claimed invention use an output supply voltage from the DC to DC converter as a supply voltage.

Fourth, Kannan fails to disclose or suggest that the discriminator (9) would provide a plurality of output signals, whether scaled or amplified. Kannan only discloses a discriminator (9) a single output signal, as shown in FIG. 1. Additionally, Kannan would have no motivation to provide output multiple signals, as Kannan is directed to a dosimeter circuit from amplifying a single ionization radiation signal detected and amplified by the detector amplifier portion shown in FIG. 3. In contrast, the claimed invention provides a plurality of outputs from both the DC to DC converter and the processing circuitry.

Finally, Kannan fails to disclose or suggest that the asserted DC to DC converter (6) and the asserted processing circuitry (9) are included in a single integrated circuit. Kannan explicitly discloses that the dosimeter of Kannan is to be constructed from "off-the-shelf" components, avoiding the use of specialty integrated circuits to keep costs low:

> [0101] A low cost radiation dose meter of the present invention is based on a silicon semiconductor diode detector has been developed. It has low power consumption leading to over 500 hours of operation without the need for changing the battery. Compared to the prior art quartz fibre electrometer based ion chamber pocket dosemeter, the present invention is more rugged, accurate and has easily readable digital display. Unlike the prior art GM counter detector based pocket dosemeters, the present invention is light in weight and is easy to carry in a shirt pocket. It is much lower in cost due to the use of readily available, off-the-shelf electronic components, than similar commercially available dosemeters which are based on a specially fabricated semiconductor detectors and Application Specific Integrated Circuits (ASICs).

In contrast, the claimed invention is a specialty integrated circuit designed to reduce the number of "off-the-shelf" components required to provide power to various integrated circuits coupled to the claimed integrated circuit in claims 1 and 17.

Accordingly, Kannan fails to disclose or suggest every feature recited in independent Claims 1 and 17 as amended. Applicant thus respectfully submits that amended Claims 1 and 17 now define over the prior art. Applicant further respectfully submits that, whereas each of the remaining dependent claims depends from one of the amended claims while reciting additional features, dependent claims likewise define over the prior art.

CONCLUSION

This application is now in full condition for allowance, which action is respectfully requested. Applicants request that the Examiner call the undersigned if clarification is needed on any matter within this Amendment, or if the Examiner believes a telephone interview would expedite the prosecution of the subject application to allowance.

Respectfully submitted,

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